Electronic Version
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Claims

[c1] 1. A method of fabricating a flash memory, comprising:
sequentially forming a tunneling dielectric layer, a first conductive layer and a mask layer on a substrate;
patterning the tunneling dielectric layer, the first conductive layer and the mask layer to form at least a strip structure;
performing an ion implantation to form a buried drain region in the substrate at one side of the strip structure;
patterning the strip structure to form a gate structure, wherein the gate structure includes the tunneling dielectric layer, the mask layer, and the first conductive layer;
forming an insulation layer adjacent to a sidewall of the gate structure, the insulation layer having a top surface lower than a top surface of the first conductive layer in a manner to expose a part of a sidewall of the first conductive layer;
forming a material layer on the insulation layer sideways adjacent to the gate structure;
removing the mask layer;
forming a second conductive layer on the top surface of the first conductive layer of the gate structure, wherein the second conductive layer covers the top surface of the

first conductive layer and further extends over the adjacent material layer;
removing the material layer to expose a part of the sidewall of the first conductive layer of the gate structure;
forming a gate dielectric layer over the the floating gate; and
forming a control gate on the gate dielectric layer.

[c2] 2. The method according to claim 1, further comprising the following steps performed after forming the second conductive layer and before removing the material layer:
(a) forming an additional material layer sideways adjacent to the floating gate, wherein the top surface of the additional material layer is lower than or approximately as high as that of the floating gate;
(b) forming an additional conductive layer on the second conductive layer of the gate structure, wherein the additional conductive layer covers the second conductive layer and further extends over the additional material layer, thereby the floating gate further includes the additional conductive layer; and
(c) removing the additional material layer.

[c3] 3. The method according to claim 2, wherein the material layers have an etching rate different from that of the insulation layer.

[c4] 4. The method according to claim 2, further comprising repeating steps (a) through (c) after forming the additional conductive layer and before removing the additional material layer.

[c5] 5. The method according to claim 1, wherein the material layer has an etching rate different from that of the insulation layer.

[c6] 6. The method according to claim 5, wherein the material of the insulation layer is silicon oxide, silicon nitride, or spin-on glass.

[c7] 7. The method according to claim 5, wherein the material layer includes either boron-phosphorus silicate glass or phosphorus silicate glass.

[c8] 8. The method according to claim 1, wherein forming the insulation layer comprises:
forming an insulation material over the substrate in a manner to cover the gate structure and fill a sideways adjacent space;
selectively removing the insulation material on the top of the gate structure to expose the mask layer; and
removing a part of the insulation material to form the insulation layer that has a top surface located at a height between a top surface and a bottom surface of the first

conductive layer of the gate structure.

[c9] 9. The method according to claim 8, wherein the step of selectively removing the insulation material on the top of the gate structure includes performing a chemical mechanical polishing (CMP) process or a back etching process.

[c10] 10. The method according to claim 8, wherein the step of removing a part of the insulation material includes performing a back etching process.

[c11] 11. A method of fabricating a flash memory, comprising:
forming a tunneling dielectric layer and a first conductive layer on a substrate;
forming a buried source/drain region in the substrate sideways adjacent to the first conductive layer;
forming an insulation layer adjacent to a sidewall of the first conductive layer, the insulation layer having a top surface located at a height between a top surface and a bottom surface of the first conductive layer;
forming a material layer on the insulation layer sideways adjacent to the first conductive layer;
forming a second conductive layer on the first conductive layer, wherein the second conductive layer covers the first conductive layer and further extends over the sideways adjacent material layer, the first and second

conductive layers thereby form a floating gate;
removing the material layer to expose a part of the sidewall of the floating gate;
forming a gate dielectric layer covering at least the exposed part of the sidewall of the floating gate; and
forming a control gate on the gate dielectric layer.

[c12] 12. The method according to claim 11, further comprising the following steps performed after forming the second conductive layer and before removing the material layer:
(a) forming an additional material layer sideways adjacent to the floating gate, wherein the top surface of the additional material layer is lower than or approximately as high as that of the floating gate;
(b) forming an additional conductive layer on the second conductive layer of the gate structure, wherein the additional conductive layer covers the second conductive layer and further extends over the additional material layer, thereby the floating gate further includes the additional conductive layer; and
(c) removing the additional material layer.

[c13] 13. The method according to claim 12, wherein the material layers have an etching rate different from that of the insulation layer.

[c14] 14. The method according to claim 12, wherein further comprising repeating steps (a) through (c) after forming the additional conductive layer and before removing the additional material layer.

[c15] 15. The method according to claim 11, wherein the material layer has an etching rate different from that of the insulation layer.

[c16] 16. The method according to claim 15, wherein the material of the insulation layer is silicon oxide, silicon nitride, or spin-on glass.

[c17] 17. The method according to claim 15, wherein the material layer includes either boron-phosphorus silicate glass or phosphorus silicate glass.

[c18] 18. The method according to claim 11, wherein forming the insulation layer comprises:
forming an insulation material over the substrate in a manner to cover the gate structure and fill a sideways adjacent space;
selectively removing the insulation material on the top of the gate structure to expose the mask layer; and
removing a part of the insulation material to form the insulation layer that has a top surface located at a height between a top surface and a bottom surface of the first

conductive layer of the gate structure.

[c19] 19. The method according to claim 18, wherein the step of selectively removing the insulation material on the top of the gate structure includes performing a chemical mechanical polishing (CMP) process or a back etching process.

[c20] 20. The method according to claim 18, wherein the step of removing a part of the insulation material includes performing a back etching process.